REMARKS

Claims 1-14, 16-20 and 23-25 are pending. Claims 1, 8, 20, and 23 are amended herein.

102(e) Rejections

Claims 1-14, 16-20, and 23-25

In paragraph 2 of the Office Action, Claims 1-14, 16-20 and 23-25 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. patent publication 2004/0019756 A1 (referred to hereinafter as "Perego"). The Applicant has reviewed the cited reference and respectfully submits that the present invention as recited in Claims 1-14, 16-20 and 23-25 is not anticipated nor rendered obvious by Perego.

Currently amended independent Claim 1 recites,

> A variable width memory system comprising:
> a bus for communicating information;
> a plurality of variable width memory locations coupled to said bus, said plurality of variable width memory locations store information, wherein said plurality of variable width memory locations receive a number of bits corresponding to the width of the variable memory locations; and
> a controller coupled to said bus, said controller directs access to said plurality of variable width memory locations, wherein said number of bits potentially varies on a per access basis depending on which variable width memory location of said plurality of variable width memory locations is being accessed.

With regard to independent Claim 1, Applicant respectfully states that Perego does not teach or suggest "wherein said number of bits potentially varies on a per access basis depending on which variable width memory location of said plurality of variable width memory locations is being accessed." For example, Perego teaches at paragraph 0004 that,

> Memory devices can be targeted to a wide variety of markets with very different sets of cost and performance constraints; consequently, the optimal device width can vary significantly from one application to the next. Unfortunately, these variations make it difficult for memory

> suppliers and distributors to accurately predict the customer demand mix for memory devices of various widths... Furthermore, a memory device manufacturer may find that optimizing the cost for each target device width means a different design at the die level and potentially at the package level. This can increase the time-to-market and level of financial and engineering resources required to deliver each of these products to market.

Further at paragraph 0012, Perego states,

> SDRAM 200 includes configuration logic 260 for setting the device width. Configuration logic 260 connects to mode register 220, and from there receives a memory width configuration value stored in register 220 during device configuration. Based on this information, configuration logic 260 configures a data control circuit 265, a latch circuit 270 and an input/output (I/O buffer 275 to obtain the device width associated with the memory-width configuration value.

Thus, Perego discloses a method for manufacturing a memory device that can be configured at the manufacturers to have different widths depending on the target device that the memory device will be shipped with. Therefore, Perego does not disclose "wherein said number of bits potentially varies on a per access basis depending on which variable width memory location of said plurality of variable width memory locations is being accessed," as recited in Claim 1.

One of the places the present application provides support for amending Claims 1, 8, 20, and 23 is at page 5, lines 18 to 24, which states:

> A variable width memory system and method utilizes variable width memory locations to store information. The variable width memory locations are accessed by referencing unique identifiers. **A precise number of bits corresponding to the width of the memory locations are transferred with each memory location access.** Thus, memory locations are not consumed in otherwise wasteful activities such as storing superfluous information.

Claims 2-7 are dependent on Claim 1 and recite additional limitations.

Applicant respectfully submits that currently amended independent Claim 8 should be patentable for similar reasons that Claim 1 should be

patentable in that Claim 8 recites, "potentially varying the bit capacity of said register on a per accesses basis to memory cells." Claims 9-19 depend on Claim 8 and recite additional limitations.

Applicant respectfully submits that currently amended independent Claim 20 should be patentable for similar reasons that Claim 1 should be patentable in that Claim 20 recites, "wherein the number of said bits potentially varies on a per accesses basis to portions of said blocks of data when identifying said bits and said width potentially varies on a per accesses basis when assigning a memory location that is equal to the number of said bits."

Applicant respectfully submits that currently amended independent Claim 23 should be patentable for similar reasons that Claim 1 should be patentable in that Claim 23 recites, "wherein the number of bits returned by said means for storing information potentially varies per read request due to which of said uniquely identifiable different width memory locations is being accessed by said read request." Claims 24 and 25 depend on Claim 23 and recite additional limitations.

Conclusions

In light of the above remarks, Applicants respectfully request reconsideration of the rejected claims.

Based on the arguments presented above, Applicants respectfully assert that Claims 1-25 overcome the rejections of record and, therefore, Applicants respectfully solicit allowance of these claims.

Applicants have reviewed the references cited but not relied upon and respectfully submit that these references neither teach nor suggest the claimed limitations.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP

Date: 8/26/04

James P. Hao
Reg. No. 36,398

Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060